Application
Note

# Kodak KSC-1000 Programming Examples - KAI-0340 Image Sensor

October 4, 2004
Revision 1.0


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## INTRODUCTION

The KSC-1000 is a programmable CCD timing generator that is designed to interface with the entire family of Kodak Interline and Full-Frame area array CCDs. The KSC-1000 uses traditional registers for defining the 13 pixel rate clocks, electronic shutter pulse generation, and general setup and control. Line Tables are used to define 6 outputs during the vertical clocking interval. Frame Tables are used to sequence the line table to create an image frame and to control portions of an imaging system. The KSC-1000 can be programmed to control image system timing or be slaved to an external controller.

This application note presents several examples of Line Table and Frame Table programming. The General Setup Register and the INTG-STRT Setup programming examples are also covered.

## LINE TABLE EXAMPLES

### I/O Mapping

The KSC-1000 line tables are used to define the states of the signals V1, V2, V3, V4, V5, and V6. These signals are used as inputs to a vertical clock driver circuit. It is assumed that a non-inverting driver circuit is used for the examples below. It is also assumed that V1 and V1C vertical clock inputs of the KAI-0340 are tied together as is shown in the KAI-0340 Device Performance Specification. The I/O map for the examples is detailed in Table 1 below. Note that two KSC-1000 outputs are required to generate the three levels required for the KAI-0340 V2 and V2C inputs.

| KSC-1000 Output | KAI-0340 Driver | Logic 1 Selection | Logic 0 Selection |
|---|---|---|---|
| V1 | V1 Driver | Mid V1 Level | Low V1 Level |
| V2 | V2 (High-Mid)-Low Drive | V2 High-Mid Driver Selection | Low V2 Level |
| V3 | V2 High-Mid Driver | High V2 Level | Mid V2 Level |
| V4 | V2C (High-Mid)-Low Driver | V2C High-Mid Driver Selection | Low V2C Level |
| V5 | V2C High-Mid Driver | High V2C Level | Mid V2C Level |
| V6 | FD Driver | High Fast Dump Level | Low Fast Dump Level |

**Table 1 KSC-1000 to KAI-0340 Vertical Clock Driver Signal Map**

Figure 1 is a copy of Timing Sequence A from the KAI-0340 Device Performance Specification. This sequence transfers the charge from all of the photodiodes to the Vertical CCD (VCCD).

## Timing Sequence A

Photodiode to VCCD transfer, entire image.

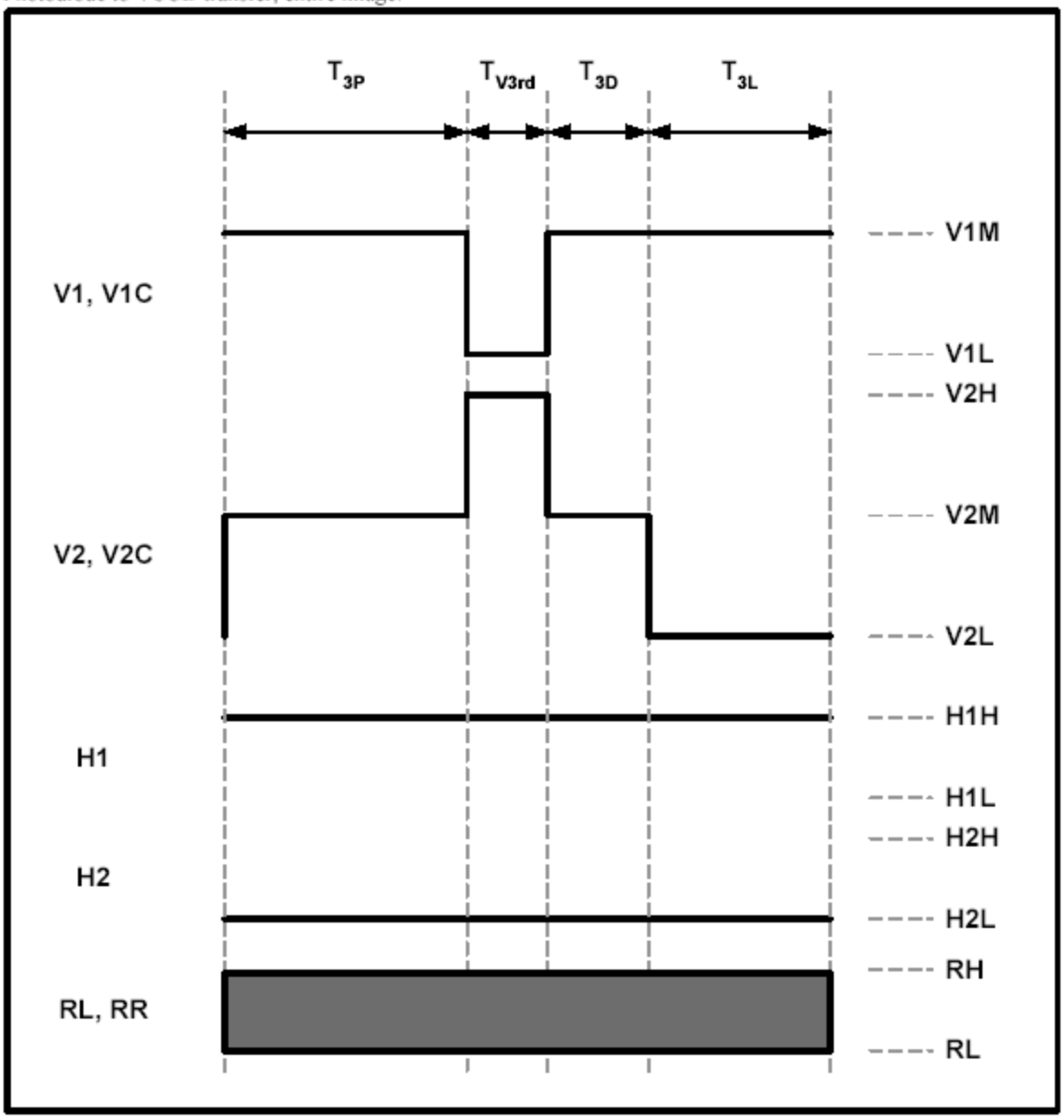


**Figure 1 KAI-0340 Timing Sequence A**

Table 2 lists the Timing Requirements for the KAI-0340. A 40MHz pixel clock frequency is assumed for the line table examples that follow. This equates to 25nS pixel period. The value in the count field is the number of pixel clock cycles that are required to produce the desired time period. For example, 8 pixel clock periods of 25nS each are required to produce the 200nS $T_{VCCD}$ time.

## AC Timing Conditions

| Description | Symbol | Minimum | Units | Notes |
|---|---|---|---|---|
| HCCD Delay | $T_{HD}$ | 200 | ns | |
| VCCD Transfer time | $T_{VCCD}$ | 200 | ns | |
| Photodiode Transfer time | $T_{V3rd}$ | 300 | ns | |
| VCCD Pedestal time | $T_{3P}$ | 15 | µs | |
| VCCD Delay | $T_{3D}$ | 5 | µs | |
| VCCD Frame Delay | $T_{3L}$ | 15 | µs | |
| VCCD Line End Delay | $T_{EL}$ | 25 | ns | |
| HCCD Clock Period | $T_{H}$ | 25 | ns | 1 |
| Reset Pulse Time | $T_{R}$ | 2.5 | ns | |
| Shutter Pulse Time | $T_{S}$ | 1.0 | µs | |
| Shutter Pulse Delay | $T_{SD}$ | 1.0 | µs | |
| Fast Line Dump Delay | $T_{FD}$ | 75 | ns | |

| Description | Symbol | Nominal | Units | Notes |
|---|---|---|---|---|
| VCCD Clock Overlap | $T_{ov}$ | 50 | % | |

**Table 2 KAI-0340 Timing Requirements**

## Line Table 0 – Timing Sequence A, Photodiode to VCCD Transfer

Table 3 is an example of a line table that implements the readout vertical clocking timing shown for Figure 1. The table uses the signal mappings described above. The line table address of 0 is an arbitrary selection. The frame table architecture permits random accessing of the line tables. The pixel clock frequency is assumed to be 40MHz, producing a 25nS pixel clock period.

| Entry | Label | Value | Time | Comment |
|---|---|---|---|---|
| 0 | Count | 600 | 15uS | 600 25nS clock periods required for a 15uS period |
| 0 | HCLK_H | 0 | | Set to 0, not last active entry in the line table |
| 0 | V6 | 0 | | FD low |
| 0 | V5 | 0 | | V2C High-Mid driver at mid level |
| 0 | V4 | 1 | | V2C driver at mid level |
| 0 | V3 | 0 | | V2 High-Mid driver at mid level |
| 0 | V2 | 1 | | V2 driver at mid level |
| 0 | V1 | 1 | | V1 driver at mid level |
| 1 | Count | 12 | 300nS | 12 25nS clock periods required for a 300nS period |
| 1 | HCLK_H | 0 | | Set to 0, not last active entry in the line table |
| 1 | V6 | 0 | | FD low |
| 1 | V5 | 1 | | V2C High-Mid driver at high level |
| 1 | V4 | 1 | | V2C driver at high level |
| 1 | V3 | 1 | | V2 High-Mid driver at high level |
| 1 | V2 | 1 | | V2 driver at high level |
| 1 | V1 | 0 | | V1 driver at low level |
| 2 | Count | 200 | 5uS | 200 25nS clock periods required for a 5uS period |
| 2 | HCLK_H | 0 | | Set to 0, not last active entry in the line table |
| 2 | V6 | 0 | | FD low |
| 2 | V5 | 0 | | V2C High-Mid driver at mid level |
| 2 | V4 | 1 | | V2C driver at mid level |
| 2 | V3 | 0 | | V2 High-Mid driver at mid level |
| 2 | V2 | 1 | | V2 driver at mid level |
| 2 | V1 | 1 | | V1 driver at mid level |

| | | | | |
|---|---|---|---|---|
| 3 | Count | 600 | 15uS | 600 25nS clock periods required for a 15uS period |
| 3 | HCLK_H | 0 | | Set to 0, do not start horizontal readout after this entry |
| 3 | V6 | 0 | | FD low |
| 3 | V5 | 0 | | V2C High-Mid driver at mid level |
| 3 | V4 | 0 | | V2C driver at low level |
| 3 | V3 | 0 | | V2 High-Mid driver at mid level |
| 3 | V2 | 0 | | V2 driver at low level |
| 3 | V1 | 1 | | V1 driver at mid level |
| 4 | Count | 0 | 0 | All zero entry to indicate end of line table |
| 4 | HCLK_H | 0 | | |
| 4 | V6 | 0 | | |
| 4 | V5 | 0 | | |
| 4 | V4 | 0 | | |
| 4 | V3 | 0 | | |
| 4 | V2 | 0 | | |
| 4 | V1 | 0 | | |

**Table 3 Line Table 0 for Photodiode to VCCD Transfer**

To program this line table, the user initiates a write to register 9, the Line Table Access Register. The 8 bit line table address is programmed next. The address consists of an entry number followed by the table number. The 5 20 bit data entries complete the bit stream for this register.

The serial data is always written LSB first. The Line Table Address needs to written 1 time only if the auto-incrementing feature of the Line Table serial interface is used. The entries are programmed in ascending order starting at the entry number specified in the Line Table Address. Program execution from a line table always starts at entry 0. The bit streams for Line Table 0 (Table 3 above) are shown in the Table 4 below.

| Register Address Label | RNW | A0 | A1 | A2 | A3 | | | |
|---|---|---|---|---|---|---|---|---|
| Register Address Bit Stream | 0 | 1 | 0 | 0 | 1 | | | |
| **Line Table Address Label** | **Entry 0** | **Address 0** | | | | | | |
| Line Table Address Bit Stream | 0000 | 0000 | | | | | | |
| **Data Entry Label** | **Count** | **HCLK_H** | **V6** | **V5** | **V4** | **V3** | **V2** | **V1** |
| Entry 0 Bit Stream | 0001101001000 | 0 | 0 | 0 | 1 | 0 | 1 | 1 |
| Entry 1 Bit Stream | 0011000000000 | 0 | 0 | 1 | 1 | 1 | 1 | 0 |
| Entry 2 Bit Stream | 0001001100000 | 0 | 0 | 0 | 1 | 0 | 1 | 1 |
| Entry 3 Bit Stream | 0001101001000 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Entry 4 Bit Stream | 0000000000000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Table 4 Line Table 0 Bit Stream**

## Line Table 1 – Timing Sequence B

Figure 2 shows the timing required to shift 1 line in the vertical CCD and readout 1 line from the horizontal CCD.

**Timing Sequence B**

Vertical CCD line shift and horizontal CCD readout of one line.

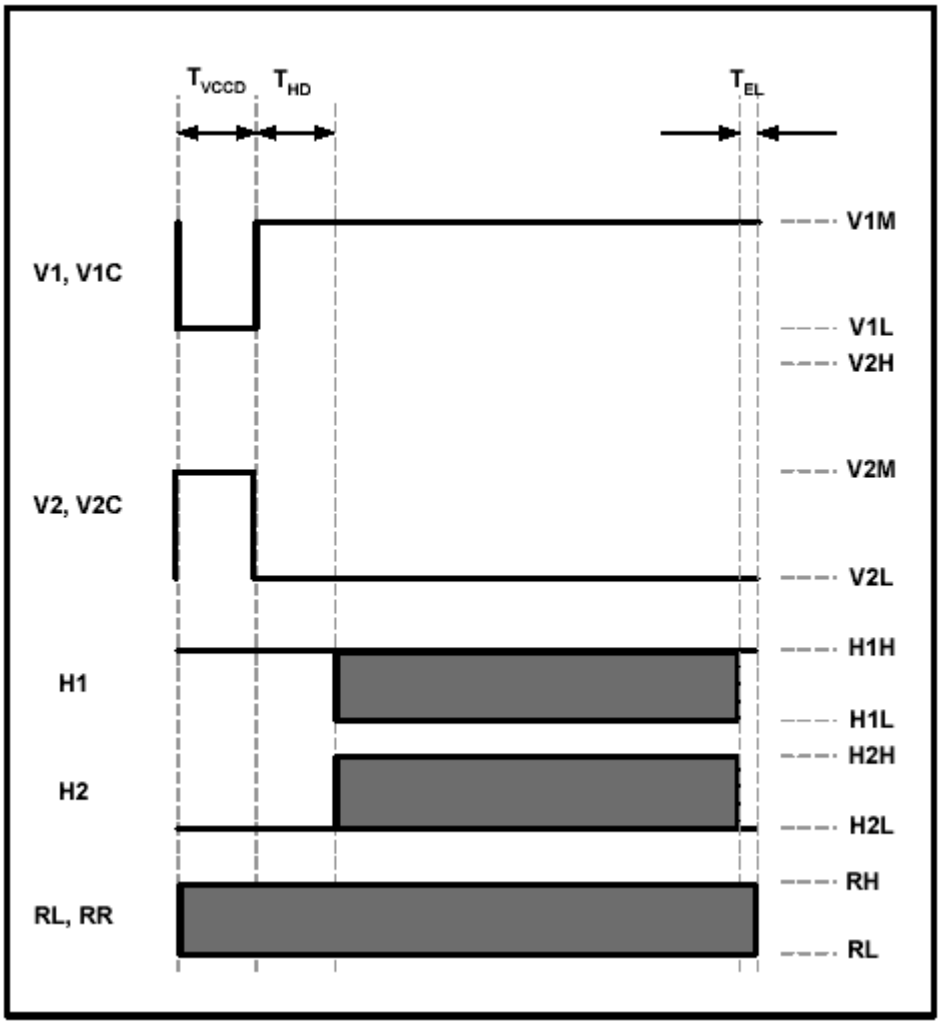


**Figure 2 Timing Sequence B**

Table 5 is an example of a line table that shows the vertical clocking sequence shown in Figure 2. This line table is assigned to address 1.

| Entry | Label | Value | Time | Comment |
|---|---|---|---|---|
| 0 | Count | 8 | 200nS | 8 25nS clock periods required for a 200nS pulse |
| 0 | HCLK_H | 0 | | Set to 0, not last active entry in the line table |
| 0 | V6 | 0 | | FD low |
| 0 | V5 | 0 | | V2C High-Mid driver at mid level |
| 0 | V4 | 1 | | V2C driver at mid level |
| 0 | V3 | 0 | | V2 High-Mid driver at mid level |
| 0 | V2 | 1 | | V2 driver at mid level |
| 0 | V1 | 0 | | V1 driver at low level |
| 1 | Count | 8 | 200nS | 8 25nS clock periods required for a 200nS period |
| 1 | HCLK_H | 1 | | Set to 1, proceed to horizontal readout upon completion of line table |
| 1 | V6 | 0 | | FD low |
| 1 | V5 | 0 | | V2C High-Mid driver at mid level |
| 1 | V4 | 0 | | V2C driver at low level |
| 1 | V3 | 0 | | V2 High-Mid driver at mid level |
| 1 | V2 | 0 | | V2 driver at low level |
| 1 | V1 | 1 | | V1 driver at mid level |
| 2 | Count | 0 | 15uS | All zero entry to indicate end of line table |
| 2 | HCLK_H | 0 | | |
| 2 | V6 | 0 | | |
| 2 | V5 | 0 | | |
| 2 | V4 | 0 | | |
| 2 | V3 | 0 | | |
| 2 | V2 | 0 | | |
| 2 | V1 | 0 | | |

**Table 5 Line Table 1 for Vertical CCD Shift and Horizontal CCD Readout.**

The serial bit stream for Line Table 1 is shown in Table 6 below:

| Register Address Label | RNW | A0 | A1 | A2 | A3 | | | |
|---|---|---|---|---|---|---|---|---|
| Register Address Bit Stream | 0 | 1 | 0 | 0 | 1 | | | |
| **Line Table Address Label** | **Entry 0** | **Address 1** | | | | | | |
| Line Table Address Bit Stream | 0000 | 1000 | | | | | | |
| **Data Entry Label** | **Count** | **HCLK_H** | **V6** | **V5** | **V4** | **V3** | **V2** | **V1** |
| Entry 0 Bit Stream | 0001000000000 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |
| Entry 1 Bit Stream | 0001000000000 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| Entry 2 Bit Stream | 0000000000000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Table 6 Line Table 1 Bit Stream**

## Line Table 2 – Timing Sequence C

Figure 3 shows the timing requirements for transferring the center 164 rows from the photodiodes to the VCCD.

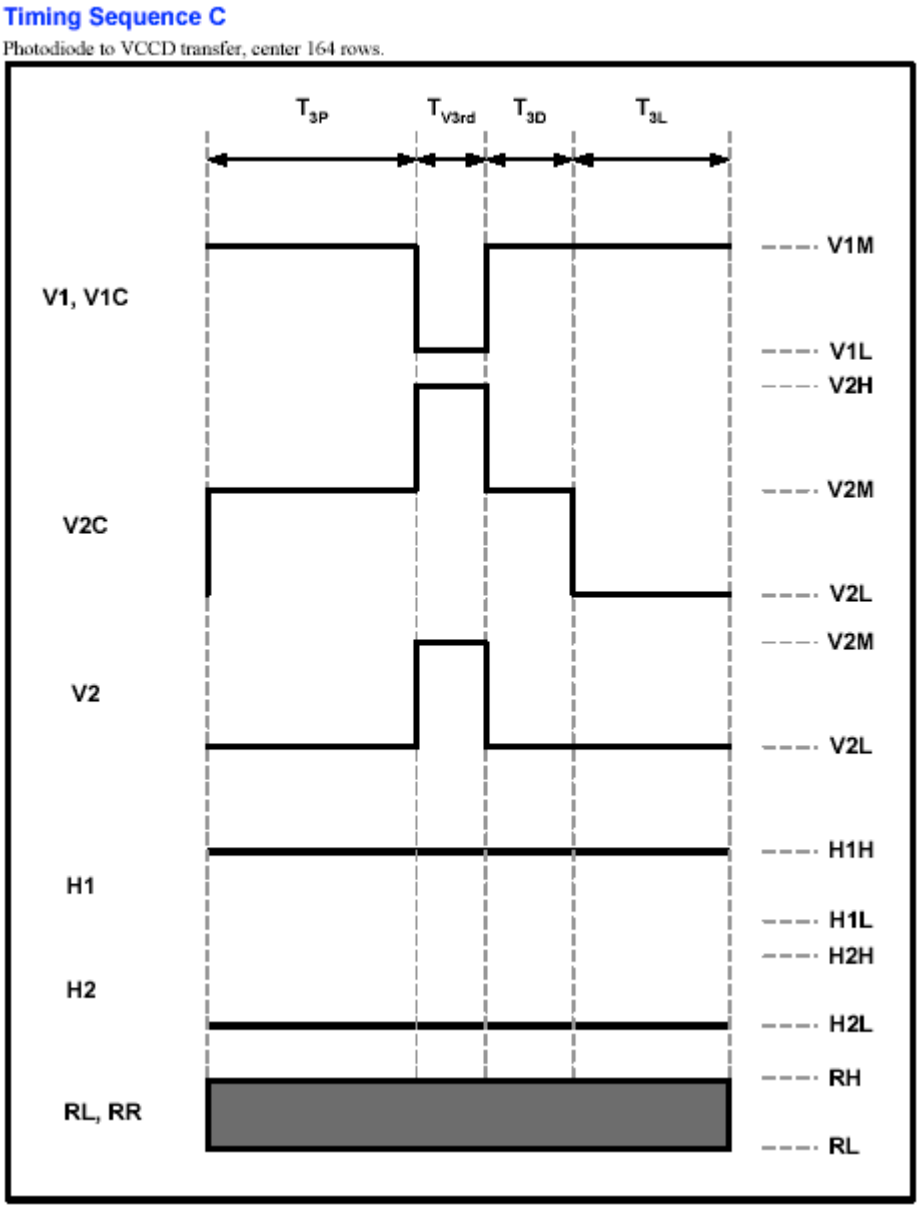


**Figure 3 Timing for Transferring 164 Center Rows to the Vertical CCD.**

Table 7 is an example of a line table that implements the center row transfer shown in Figure 3. This line table is assigned to address 2.

| Entry | Label | Value | Time | Comment |
|---|---|---|---|---|
| 0 | Count | 600 | 15uS | 600 25nS clock periods required for a 15uS pulse |
| 0 | HCLK_H | 0 | | Set to 0, not last active entry in the line table |
| 0 | V6 | 1 | | FD high |
| 0 | V5 | 0 | | V2C High-Mid driver at mid level |
| 0 | V4 | 1 | | V2C driver at mid level |
| 0 | V3 | 0 | | V2 High-Mid driver at mid level |
| 0 | V2 | 0 | | V2 driver at low level |
| 0 | V1 | 1 | | V1 driver at mid level |
| 1 | Count | 12 | 300nS | 12 25nS clock periods required for a 300nS pulse |
| 1 | HCLK_H | 0 | | Set to 0, not last active entry in the line table |
| 1 | V6 | 1 | | FD high |
| 1 | V5 | 1 | | V2C High-Mid driver at high level |
| 1 | V4 | 1 | | V2C driver at high level |
| 1 | V3 | 0 | | V2 High-Mid driver at mid level |
| 1 | V2 | 1 | | V2 driver at mid level |
| 1 | V1 | 0 | | V1 driver at low level |
| 2 | Count | 200 | 5uS | 200 25nS clock periods required for a 5uS pulse |
| 2 | HCLK_H | 0 | | Set to 0, not last active entry in the line table |
| 2 | V6 | 1 | | FD high |
| 2 | V5 | 0 | | V2C High-Mid driver at mid level |
| 2 | V4 | 1 | | V2C driver at mid level |
| 2 | V3 | 0 | | V2 High-Mid driver at mid level |
| 2 | V2 | 0 | | V2 driver at low level |
| 2 | V1 | 1 | | V1 driver at mid level |
| 3 | Count | 600 | 15uS | 600 25nS clock periods required for a 15uS pulse |
| 3 | HCLK_H | 0 | | Set to 0, do not start horizontal readout after this entry |
| 3 | V6 | 1 | | FD high |
| 3 | V5 | 0 | | V2C High-Mid driver at mid level |
| 3 | V4 | 0 | | V2C driver at low level |
| 3 | V3 | 0 | | V2 High-Mid driver at mid level |
| 3 | V2 | 0 | | V2 driver at low level |
| 3 | V1 | 1 | | V1 driver at mid level |

| | | | | |
|---|---|---|---|---|
| 4 | Count | 0 | 0 | All zero entry to indicate end of line table |
| 4 | HCLK_H | 0 | | |
| 4 | V6 | 0 | | |
| 4 | V5 | 0 | | |
| 4 | V4 | 0 | | |
| 4 | V3 | 0 | | |
| 4 | V2 | 0 | | |
| 4 | V1 | 0 | | |

**Table 7 Line Table 2 Center Row Readout Timing**

The serial bit stream for Line Table 2 is shown in Table 8 below

| Register Address Label | RNW | A0 | A1 | A2 | A3 | | | |
|---|---|---|---|---|---|---|---|---|
| Register Address Bit Stream | 0 | 1 | 0 | 0 | 1 | | | |
| **Line Table Address Label** | **Entry 0** | **Address 2** | | | | | | |
| Line Table Address Bit Stream | 0000 | 0100 | | | | | | |
| **Data Entry Label** | **Count** | **HCLK_H** | **V6** | **V5** | **V4** | **V3** | **V2** | **V1** |
| Entry 0 Bit Stream | 0001101001000 | 0 | 1 | 0 | 1 | 0 | 0 | 1 |
| Entry 1 Bit Stream | 0011000000000 | 0 | 1 | 1 | 1 | 0 | 1 | 0 |
| Entry 2 Bit Stream | 0001001100000 | 0 | 1 | 0 | 1 | 0 | 0 | 1 |
| Entry 3 Bit Stream | 0001101001000 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| Entry 4 Bit Stream | 0000000000000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Table 8 Line Table 2 Serial Bit Stream**

## Line Table 3 – Timing Sequence D

Figure 4 shows the timing requirements for clocking out the horizontal CCD with no vertical CCD clocking. This clocking sequence is used for the center column readout modes of the KAI-0340.

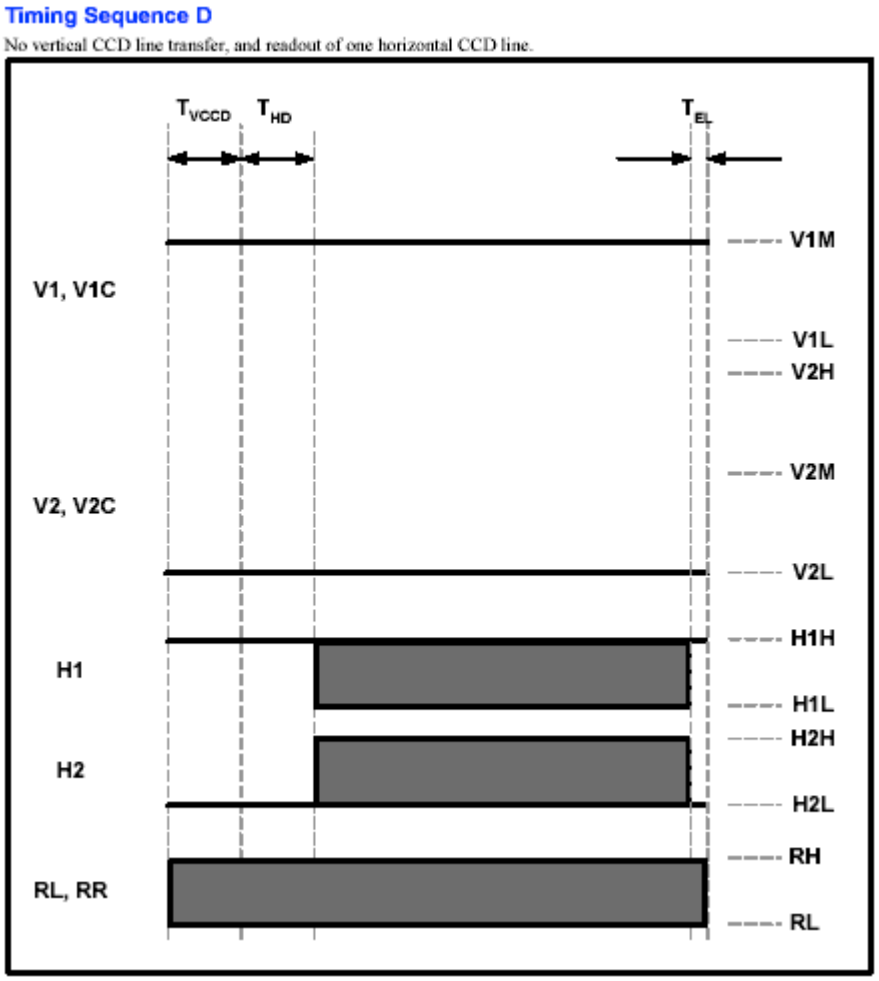


**Figure 4 Timing Sequence D, Horizontal Readout with no Vertical Clock**

Table 9 is an example of a line table that shows the vertical clocking sequence shown in Figure 4. This line table is assigned to address 3. In this case the $T_{EL}$, $T_{VCCD}$, and $T_{HD}$ periods can be combined into a single period since no state changes occur. $T_{EL}$ can be considered the first event in the vertical interval. Therefore the total time for the $T_{EL}$, $T_{VCCD}$, and $T_{HD}$ periods is 425nS.

| Entry | Label | Value | Time | Comment |
|---|---|---|---|---|
| 0 | Count | 9 | 425nS | 9 25nS clock periods required for a 425nS period |
| 0 | HCLK_H | 1 | | Set to 1, proceed to horizontal readout upon completion of line table |
| 0 | V6 | 1 | | FD high |
| 0 | V5 | 0 | | V2C High-Mid driver at mid level |
| 0 | V4 | 0 | | V2C driver at low level |
| 0 | V3 | 0 | | V2 High-Mid driver at mid level |
| 0 | V2 | 0 | | V2 driver at low level |
| 0 | V1 | 1 | | V1 driver at mid level |
| 1 | Count | 0 | 0 | All zero entry to indicate end of line table |
| 1 | HCLK_H | 0 | | |
| 1 | V6 | 0 | | |
| 1 | V5 | 0 | | |
| 1 | V4 | 0 | | |
| 1 | V3 | 0 | | |
| 1 | V2 | 0 | | |
| 1 | V1 | 0 | | |

**Table 9 Line Table 3 Horizontal Readout with no Vertical Clocking**

The serial bit stream for Line Table 3 is shown in Table 10 below:

| Register Address Label | RNW | A0 | A1 | A2 | A3 | | | |
|---|---|---|---|---|---|---|---|---|
| Register Address Bit Stream | 0 | 1 | 0 | 0 | 1 | | | |
| **Line Table Address Label** | **Entry 0** | **Address 3** | | | | | | |
| Line Table Address Bit Stream | 0000 | 1100 | | | | | | |
| **Data Entry Label** | **Count** | **HCLK_H** | **V6** | **V5** | **V4** | **V3** | **V2** | **V1** |
| Entry 0 Bit Stream | 1001000000000 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| Entry 1 Bit Stream | 0000000000000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Table 10 Line Table 3 Serial Bit Stream**

## Line Table 4 – Idle State

An idle state will be used to allow reprogramming of the General Setup register. This register will need to be reprogrammed when switching between center column readout and full image readout. This line table holds V2 and V2C at the $V_{2L}$ level and holds V1 and V1C at the $V_{1M}$ level. The horizontal readout state will not entered upon completion of the line table. A period of 18.165uS, which corresponds to a full image single readout line time is arbitrarily chosen. The idle state line table can be called repeatedly until the programming cycle is completed.

| Entry | Label | Value | Time | Comment |
|---|---|---|---|---|
| 0 | Count | 746 | 18.165u | 746 25nS clock periods required for a 18.165uS period |
| 0 | HCLK_H | 0 | | Set to 0, do not start horizontal readout upon completion of line table |
| 0 | V6 | 0 | | FD low |
| 0 | V5 | 0 | | V2C High-Mid driver at mid level |
| 0 | V4 | 0 | | V2C driver at low level |
| 0 | V3 | 0 | | V2 High-Mid driver at mid level |
| 0 | V2 | 0 | | V2 driver at low level |
| 0 | V1 | 1 | | V1 driver at mid level |
| 1 | Count | 0 | 0 | All zero entry to indicate end of line table |
| 1 | HCLK_H | 0 | | |
| 1 | V6 | 0 | | |
| 1 | V5 | 0 | | |
| 1 | V4 | 0 | | |
| 1 | V3 | 0 | | |
| 1 | V2 | 0 | | |
| 1 | V1 | 0 | | |

**Table 11 Line Table 4 Idle State Timing**

The serial bit stream for Line Table 4 is shown in Table 12 below:

| Register Address Label | RNW | A0 | A1 | A2 | A3 | | | |
|---|---|---|---|---|---|---|---|---|
| Register Address Bit Stream | 0 | 1 | 0 | 0 | 1 | | | |
| **Line Table Address Label** | **Entry 0** | **Address 4** | | | | | | |
| Line Table Address Bit Stream | 0000 | 0010 | | | | | | |
| **Data Entry Label** | **Count** | **HCLK_H** | **V6** | **V5** | **V4** | **V3** | **V2** | **V1** |
| Entry 0 Bit Stream | 0101011101000 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Entry 1 Bit Stream | 0000000000000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Table 12 Line Table 4 Serial Bit Stream**

## Line Table 5 – Timing Sequence B with Fast Dump Asserted

For Center Column readout, the FD pin needs to held at the Fast Dump high level to prevent charge from the outer columns from being transferred into the Vertical CCD. The FDC pin is held at the Fast Dump low level to allow charge from the center columns to be transferred to the Vertical CCD.

Table 13 is an example of a line table that shows the vertical clocking sequence shown in Figure 2 with the FD Line asserted. This line table is assigned to address 5.

| Entry | Label | Value | Time | Comment |
|---|---|---|---|---|
| 0 | Count | 3 | 75nS | 3 25nS clock periods required for a 75nS $T_{FD}$ period |
| 0 | HCLK_H | 0 | | Set to 0, not last active entry in the line table |
| 0 | V6 | 1 | | FD high |
| 0 | V5 | 0 | | V2C High-Mid driver at mid level |
| 0 | V4 | 0 | | V2C driver at mid level |
| 0 | V3 | 0 | | V2 High-Mid driver at mid level |
| 0 | V2 | 0 | | V2 driver at mid level |
| 0 | V1 | 1 | | V1 driver at low level |
| 1 | Count | 8 | 200nS | 8 25nS clock periods required for a 200nS pulse |
| 1 | HCLK_H | 0 | | Set to 0, not last active entry in the line table |
| 1 | V6 | 1 | | FD high |
| 1 | V5 | 0 | | V2C High-Mid driver at mid level |
| 1 | V4 | 1 | | V2C driver at mid level |
| 1 | V3 | 0 | | V2 High-Mid driver at mid level |
| 1 | V2 | 1 | | V2 driver at mid level |
| 1 | V1 | 0 | | V1 driver at low level |
| 2 | Count | 8 | 200nS | 8 25nS clock periods required for a 200nS period |
| 2 | HCLK_H | 1 | | Set to 1, proceed to horizontal readout upon completion of line table |
| 2 | V6 | 1 | | FD high |
| 2 | V5 | 0 | | V2C High-Mid driver at mid level |
| 2 | V4 | 0 | | V2C driver at low level |
| 2 | V3 | 0 | | V2 High-Mid driver at mid level |
| 2 | V2 | 0 | | V2 driver at low level |
| 2 | V1 | 1 | | V1 driver at mid level |

| | | | | |
|---|---|---|---|---|
| 3 | Count | 0 | 15uS | All zero entry to indicate end of line table |
| 3 | HCLK_H | 0 | | |
| 3 | V6 | 0 | | |
| 3 | V5 | 0 | | |
| 3 | V4 | 0 | | |
| 3 | V3 | 0 | | |
| 3 | V2 | 0 | | |
| 3 | V1 | 0 | | |

**Table 13 Line Table 5 Timing Sequence B with Fast Dump Asserted**

The serial bit stream for Line Table 5 is shown in Table 14 below:

| Register Address Label | RNW | A0 | A1 | A2 | A3 | | | |
|---|---|---|---|---|---|---|---|---|
| Register Address Bit Stream | 0 | 1 | 0 | 0 | 1 | | | |
| **Line Table Address Label** | **Entry 0** | **Address 5** | | | | | | |
| Line Table Address Bit Stream | 0000 | 1010 | | | | | | |
| **Data Entry Label** | **Count** | **HCLK_H** | **V6** | **V5** | **V4** | **V3** | **V2** | **V1** |
| Entry 0 Bit Stream | 1100000000000 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| Entry 1 Bit Stream | 0001000000000 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| Entry 32Bit Stream | 0001000000000 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| Entry 3 Bit Stream | 0000000000000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Table 14 Line Table 5 Serial Bit Stream**

## FRAME TABLE EXAMPLES

Frame Tables are used to link together a sequence of line tables. The following examples switch between Single Output Full Image Capture and Single Output Center Rows and Columns Readout modes. Frame Table 0 is configured for a Single Output Center Rows and Columns Readout sequence. Frame Table 1 is configured for an Idle State. The idle state is used to allow the imaging system to be programmed for another mode. Frame Table 2 is configured for a Single Output Full Image Capture event. The VD event is used to switch from Frame Table 0 to Frame Table 1 and from Frame Table 1 to Frame Table 2..

### Frame Table 0

Entry 0 is an example of the ExLT command. This entry calls Line Table 2. That Line Table is used to transfer charge from the center 164 rows to the Vertical CCD. The first line of charge is also transferred to the Horizontal CCD. This entry also clears the vertical line counter. All clamping is disabled in this entry. Frame Valid, Line Valid, and PBLK are disabled. The vertical line counter is cleared in this entry.

| Label | Value | Comment |
|---|---|---|
| Check and Increment Line Counter | 0 | Do not increment Line Counter or compare with INTG_STRT Line Register |
| Clear Line Counter | 1 | Clear Line Counter |
| Force INTG_STRT | 0 | Do not force INTG_STRT |
| Horizontal Binning Factor | 0 | No Binning |
| HCLK_V Enable | 0 | Do not enable HCLKS during Vertical Interval |
| Line Valid Enable | 0 | Disable Line Valid |
| Frame Valid Enable | 0 | Disable Frame Valid |
| Video Amplifier Enable | 1 | Enable Video Amplifier |
| AFE Clock Enable | 1 | Enable AFE Clocks |
| CLPDM2 Enable | 0 | Disable Line Rate clamp |
| CLPDM1 Enable | 0 | Disable Frame Rate clamp |
| CLPOB2 Enable | 0 | Disable Line Rate clamp |
| CLPOB1 Enable | 0 | Disable Frame Rate clamp |
| PBLK Enable | 0 | Disable PBLK |
| PBLK Idle Val | 1 | PBLK active low |
| Flag | 0 | |
| Count | 1 | Execute Line Table 2 1X, proceed to next entry when finished |
| Address 2:0 | 2 | |
| Address 3 | 0 | |

**Table 15 Frame Table 0, Entry 0**

Entry 1 is another example of the ExLT command. This entry calls Line Table 3. This line table does not clock the Vertical CCD. Horizontal readout is enabled after completion of this line table. The Pixels Per Line field of the General Setup Register is programmed to a value of 246. This count produces 18 over clocked pixels at the end of each line that can be used for clamping. The vertical line counter is enabled for this line. The frame rate clamps and PBLK are disabled. The line rate clamps are disabled. Frame Valid and Line Valid are disabled.

| Label | Value | Comment |
|---|---|---|
| Check and Increment Line Counter | 1 | Increment Line Counter and compare with INTG_STRT Line Register |
| Clear Line Counter | 0 | Do not clear Line Counter |
| Force INTG_STRT | 0 | Do not force INTG_STRT |
| Horizontal Binning Factor | 0 | No Binning |
| HCLK_V Enable | 0 | Do not enable HCLKS during Vertical Interval |
| Line Valid Enable | 0 | Disable Line Valid |
| Frame Valid Enable | 0 | Disable Frame Valid |
| Video Amplifier Enable | 1 | Enable Video Amplifier |
| AFE Clock Enable | 1 | Enable AFE Clocks |
| CLPDM2 Enable | 0 | Disable Line Rate clamp |
| CLPDM1 Enable | 0 | Disable Frame Rate clamp |
| CLPOB2 Enable | 0 | Disable Line Rate clamp |
| CLPOB1 Enable | 0 | Disable Frame Rate clamp |
| PBLK Enable | 0 | Disable PBLK |
| PBLK Idle Val | 1 | PBLK active low |
| Flag | 0 | |
| Count | 1 | Execute Line Table 3 1x, proceed to next entry when finished |
| Address 2:0 | 3 | |
| Address 3 | 0 | |

**Table 16 Frame Table 0, Entry 1**

Entry 2 implements the ExLT command. This entry calls Line Table 5. This table generates a standard vertical clock sequence that clocks out all 164 center rows. The vertical line counter is enabled for this line. The frame rate clamps are disabled while the line rate clamps are enabled. Frame Valid and Line Valid are enabled. PBLK is disabled.

| Label | Value | Comment |
|---|---|---|
| Check and Increment Line Counter | 1 | Increment Line Counter and compare with INTG_STRT Line Register |
| Clear Line Counter | 0 | Do not clear Line Counter |
| Force INTG_STRT | 0 | Do not force INTG_STRT |
| Horizontal Binning Factor | 0 | No Binning |
| HCLK_V Enable | 0 | Do not enable HCLKS during Vertical Interval |
| Line Valid Enable | 1 | Enable Line Valid |
| Frame Valid Enable | 1 | Enable Frame Valid |
| Video Amplifier Enable | 1 | Enable Video Amplifier |
| AFE Clock Enable | 1 | Enable AFE Clocks |
| CLPDM2 Enable | 1 | Enable Line Rate clamp |
| CLPDM1 Enable | 0 | Disable Frame Rate clamp |
| CLPOB2 Enable | 1 | Enable Line Rate clamp |
| CLPOB1 Enable | 0 | Disable Frame Rate clamp |
| PBLK Enable | 0 | Disable PBLK |
| PBLK Idle Val | 1 | PBLK active low |
| Flag | 0 | |
| Count | 163 | Execute Line Table 5 163x, proceed to next entry when finished |
| Address 2:0 | 5 | |
| Address 3 | 0 | |

**Table 17 Frame Table 0, Entry 2**

Entry 3 implements ExLT command again. This entry calls line table 3. This line table does not clock the Vertical CCD. Horizontal readout is enabled after completion of this line table. This entry produces 4 over clocked lines that are used for frame rate clamping. Line Valid, Frame Valid, and PBLK are disabled. Frame rate clamping is enabled while line rate clamping is disabled.

| Label | Value | Comment |
|---|---|---|
| Check and Increment Line Counter | 1 | Increment Line Counter and compare with INTG_STRT Line Register |
| Clear Line Counter | 0 | Do not clear Line Counter |
| Force INTG_STRT | 0 | Do not force INTG_STRT |
| Horizontal Binning Factor | 0 | No Binning |
| HCLK_V Enable | 0 | Do not enable HCLKS during Vertical Interval |
| Line Valid Enable | 0 | Disable Line Valid |
| Frame Valid Enable | 0 | Disable Frame Valid |
| Video Amplifier Enable | 1 | Enable Video Amplifier |
| AFE Clock Enable | 1 | Enable AFE Clocks |
| CLPDM2 Enable | 0 | Disable Line Rate clamp |
| CLPDM1 Enable | 1 | Enable Frame Rate clamp |
| CLPOB2 Enable | 0 | Disable Line Rate clamp |
| CLPOB1 Enable | 1 | Enable Frame Rate clamp |
| PBLK Enable | 0 | Disable PBLK |
| PBLK Idle Val | 1 | PBLK active low |
| Flag | 0 | |
| Count | 4 | Execute Line Table 3 4x, proceed to next entry when finished |
| Address 2:0 | 3 | |
| Address 3 | 0 | |

**Table 18 Frame Table 0, Entry 3**

Entry 4 is an implementation of the JmpFTVD command. If a VD event has been registered, control jumps to Frame Table 1 to enter the Idle State. Otherwise, operation continues with Entry 5 in this Frame Table. Signals that are activated at programmed pixel counts such as PBLK, line valid, frame valid, frame rate clamps, and line rate clamps are not activated with this command regardless of the state of the control bit. Only the ExLT or the ExLTNVD commands directly execute line tables which in turn can start the horizontal state machine.

| Label | Value | Comment |
|---|---|---|
| Check and Increment Line Counter | 0 | Increment Line Counter and compare with INTG_STRT Line Register |
| Clear Line Counter | 0 | Do not clear Line Counter |
| Force INTG_STRT | 0 | Do not force INTG_STRT |
| Horizontal Binning Factor | 0 | No Binning |
| HCLK_V Enable | 0 | Do not enable HCLKS during Vertical Interval |
| Line Valid Enable | 0 | Disable Line Valid |
| Frame Valid Enable | 0 | Disable Frame Valid |
| Video Amplifier Enable | 1 | Enable Video Amplifier |
| AFE Clock Enable | 1 | Enable AFE Clocks |
| CLPDM2 Enable | 0 | Disable Line Rate clamp |
| CLPDM1 Enable | 0 | Disable Frame Rate clamp |
| CLPOB2 Enable | 0 | Disable Line Rate clamp |
| CLPOB1 Enable | 0 | Disable Frame Rate clamp |
| PBLK Enable | 0 | Disable PBLK |
| PBLK Idle Val | 1 | PBLK active low |
| Flag | 0 | |
| Count | 0 | Jump to Entry 0 of Frame Table 1 if a VD event has been registered. Continue operation with Entry 5 of Frame Table 0 if no VD event has been registered. |
| Address 2:0 | 1 | |
| Address 3 | 1 | |

**Table 19 Frame Table 0, Entry 4**

Entry 5 is an example of the JmpFT command. Control jumps back to entry 0 of this Frame Table. This architecture provides a continuous capture loop. Entry 4 provides an escape from the continuous loop when an external controller provides a VD signal. Signals that are activated at programmed pixel counts such as PBLK, line valid, frame valid, frame rate clamps, and line rate clamps are not activated with this command regardless of the state of the control bit. Only the ExLT or the ExLTNVD commands directly execute line tables which in turn can start the horizontal state machine.

| Label | Value | Comment |
|---|---|---|
| Check and Increment Line Counter | 0 | Do not increment Line Counter or compare with INTG_STRT Line Register |
| Clear Line Counter | 0 | Do not clear Line Counter |
| Force INTG_STRT | 0 | Do not force INTG_STRT |
| Horizontal Binning Factor | 0 | No Binning |
| HCLK_V Enable | 0 | Do not enable HCLKS during Vertical Interval |
| Line Valid Enable | 0 | Do not Enable Line Valid |
| Frame Valid Enable | 0 | Do not enable Frame Valid |
| Video Amplifier Enable | 1 | Enable Video Amplifier |
| AFE Clock Enable | 1 | Enable AFE Clocks |
| CLPDM2 Enable | 0 | Disable Line Rate clamp |
| CLPDM1 Enable | 0 | Disable Frame Rate clamp |
| CLPOB2 Enable | 0 | Disable Line Rate clamp |
| CLPOB1 Enable | 0 | Disable Frame Rate clamp |
| PBLK Enable | 0 | Set PBLK high |
| PBLK Idle Val | 1 | PBLK active low |
| Flag | 0 | |
| Count | 0 | Jump to Entry 0 of Frame Table 0 |
| Address 2:0 | 0 | |
| Address 3 | 0 | |

**Table 20 Frame Table 0, Entry 5**

To program Frame Table 0, the user initiates a write to register 8, the Frame Table Access Register. The 7 bit frame table address is programmed next. The address consists of an entry number followed by the table number. The 7 34 bit data entries complete the bit stream for this register.

The serial data is always written LSB first. The Frame Table Address needs to written 1 time only if the auto-incrementing feature of the Line Table serial interface is used. The entries are programmed in ascending order starting at the entry number specified in the Line Table Address. Program execution from a frame table always starts at entry 0. The bit streams for Frame Table 0 are shown in the Table 16 below.

Some of the individual control bits have been grouped in the table below. The INTG_STRT Cntl field consists of the Check and Increment Line Counter Bit (LSB), followed by Clear Line Counter Bit and the Force INTG_START bit in that order. The H Bin field consists of 2 bits. The Enables field consists of the HCLK_V Enable bit (LSB) followed by the Line Valid Enable bit, the Frame Valid Enable bit, the Video Amplifier Enable bit, the AFE Clock Enable bit, the CLPDM2 Enable bit, the CLPDM1 Enable bit, the CLPOB2 Enable bit, the CLPOB1 Enable bit, and the PBLK enable bit in that order. The count field contains 13 bits.

| Register Address Label | RNW | A0 | A1 | A2 | A3 | | | |
|---|---|---|---|---|---|---|---|---|
| Register Address Bit Stream | 0 | 0 | 0 | 0 | 1 | | | |
| **Line Table Address Label** | **Entry 0** | **Addr 0** | | | | | | |
| Line Table Address Bit Stream | 0000 | 000 | | | | | | |
| **Data Entry Label** | **INTG_STRT Cntl** | **H Bin** | **Enables** | **PBLK Idle** | **Flag** | **Count** | **A0:2** | **A3** |
| Entry 0 Bit Stream | 010 | 00 | 000110000( | 1 | 0 | 1000000000000 | 01( | 0 |
| Entry 1 Bit Stream | 100 | 00 | 000110000( | 1 | 0 | 1000000000000 | 11( | 0 |
| Entry 2 Bit Stream | 100 | 00 | 011111010( | 1 | 0 | 1100010100000 | 101 | 0 |
| Entry 3 Bit Stream | 100 | 00 | 000110101( | 1 | 0 | 0010000000000 | 11( | 0 |
| Entry 4 Bit Stream | 000 | 00 | 000110000( | 1 | 0 | 0000000000000 | 10( | 1 |
| Entry 5 Bit Stream | 000 | 00 | 000110000( | 1 | 0 | 0000000000000 | 00( | 0 |

**Table 21 Frame Table 0 Serial Bit Stream**

## Frame Table 1

Frame Table 1 implements the Idle State. Line Table 4 maintains inactive vertical clocks for a period of 18.165uS. This is the time required to clock out 1 horizontal line in the Single Output Full Image Readout mode. Horizontal Readout is not triggered after completion of the line table. The vertical counter, Frame Rate clamp, Line Rate clamp, Frame Valid, Line Valid, and PBLK are all disabled in Frame Table 1.

Frame Table 1 uses the VD event to control mode switching. Entry 0 uses the ExLTNVD instruction to call Line Table 4 repeatedly until the external controller generates a VD signal. The external controller can use the Idle State to reprogram the General Control Register to set up for the Single Output Full Image Capture mode. Once the VD event is detected, execution of Line Table 4 is completed and program control is passed on to Entry 1.

| Label | Value | Comment |
|---|---|---|
| Check and Increment Line Counter | 0 | Do not increment Line Counter or compare with INTG_STRT Line Register |
| Clear Line Counter | 0 | Do not Clear Line Counter |
| Force INTG_STRT | 0 | Do not force INTG_STRT |
| Horizontal Binning Factor | 0 | No Binning |
| HCLK_V Enable | 0 | Do not enable HCLKS during Vertical Interval |
| Line Valid Enable | 0 | Disable Line Valid |
| Frame Valid Enable | 0 | Disable Frame Valid |
| Video Amplifier Enable | 1 | Enable Video Amplifier |
| AFE Clock Enable | 1 | Enable AFE Clocks |
| CLPDM2 Enable | 0 | Disable Line Rate clamp |
| CLPDM1 Enable | 0 | Disable Frame Rate clamp |
| CLPOB2 Enable | 0 | Disable Line Rate clamp |
| CLPOB1 Enable | 0 | Disable Frame Rate clamp |
| PBLK Enable | 0 | Disable PBLK |
| PBLK Idle Val | 1 | PBLK active low |
| Flag | 1 | |
| Count | 0 | Execute Line Table 4 repeatedly until a VD event is detected. |
| Address 2:0 | 4 | |
| Address 3 | 0 | |

**Table 22 Frame Table 1, Entry 0**

Entry 1 is an ExLT instruction. The Idle State is called one more time to allow the external controller to generate an additional VD signal if the control is to be passed to Frame Table 2. In the event that no VD signal is generated, control is passed back to Frame Table 0.

| Label | Value | Comment |
|---|---|---|
| Check and Increment Line Counter | 0 | Do not increment Line Counter or compare with INTG_STRT Line Register |
| Clear Line Counter | 0 | Do not Clear Line Counter |
| Force INTG_STRT | 0 | Do not force INTG_STRT |
| Horizontal Binning Factor | 0 | No Binning |
| HCLK_V Enable | 0 | Do not enable HCLKS during Vertical Interval |
| Line Valid Enable | 0 | Disable Line Valid |
| Frame Valid Enable | 0 | Disable Frame Valid |
| Video Amplifier Enable | 1 | Enable Video Amplifier |
| AFE Clock Enable | 1 | Enable AFE Clocks |
| CLPDM2 Enable | 0 | Disable Line Rate clamp |
| CLPDM1 Enable | 0 | Disable Frame Rate clamp |
| CLPOB2 Enable | 0 | Disable Line Rate clamp |
| CLPOB1 Enable | 0 | Disable Frame Rate clamp |
| PBLK Enable | 0 | Disable PBLK |
| PBLK Idle Val | 1 | PBLK active low |
| Flag | 0 | |
| Count | 1 | Execute Line Table 4 1x. |
| Address 2:0 | 4 | |
| Address 3 | 0 | |

**Table 23 Frame Table 1, Entry 1**

Entry 2 is a JmpFTVD instruction. If a VD signal was detected, control is passed to Frame Table 2 Entry 0 to start the Single Output Full Image Capture mode. Otherwise, entry 3 is executed.

| Label | Value | Comment |
|---|---|---|
| Check and Increment Line Counter | 0 | Do not increment Line Counter or compare with INTG_STRT Line Register |
| Clear Line Counter | 0 | Do not Clear Line Counter |
| Force INTG_STRT | 0 | Do not force INTG_STRT |
| Horizontal Binning Factor | 0 | No Binning |
| HCLK_V Enable | 0 | Do not enable HCLKS during Vertical Interval |
| Line Valid Enable | 0 | Disable Line Valid |
| Frame Valid Enable | 0 | Disable Frame Valid |
| Video Amplifier Enable | 1 | Enable Video Amplifier |
| AFE Clock Enable | 1 | Enable AFE Clocks |
| CLPDM2 Enable | 0 | Disable Line Rate clamp |
| CLPDM1 Enable | 0 | Disable Frame Rate clamp |
| CLPOB2 Enable | 0 | Disable Line Rate clamp |
| CLPOB1 Enable | 0 | Disable Frame Rate clamp |
| PBLK Enable | 0 | Disable PBLK |
| PBLK Idle Val | 1 | PBLK active low |
| Flag | 0 | |
| Count | 0 | Jump to Frame Table 2 Entry 0. |
| Address 2:0 | 2 | |
| Address 3 | 1 | |

**Table 24 Frame Table 1, Entry 2**

Entry 3 is a JmpFT instruction. Control is passed to Frame Table 0.

| Label | Value | Comment |
|---|---|---|
| Check and Increment Line Counter | 0 | Do not increment Line Counter or compare with INTG_STRT Line Register |
| Clear Line Counter | 0 | Do not Clear Line Counter |
| Force INTG_STRT | 0 | Do not force INTG_STRT |
| Horizontal Binning Factor | 0 | No Binning |
| HCLK_V Enable | 0 | Do not enable HCLKS during Vertical Interval |
| Line Valid Enable | 0 | Disable Line Valid |
| Frame Valid Enable | 0 | Disable Frame Valid |
| Video Amplifier Enable | 1 | Enable Video Amplifier |
| AFE Clock Enable | 1 | Enable AFE Clocks |
| CLPDM2 Enable | 0 | Disable Line Rate clamp |
| CLPDM1 Enable | 0 | Disable Frame Rate clamp |
| CLPOB2 Enable | 0 | Disable Line Rate clamp |
| CLPOB1 Enable | 0 | Disable Frame Rate clamp |
| PBLK Enable | 0 | Disable PBLK |
| PBLK Idle Val | 1 | PBLK active low |
| Flag | 0 | |
| Count | 0 | Jump to Frame Table 0 Entry 0. |
| Address 2:0 | 0 | |
| Address 3 | 0 | |

**Table 25 Frame Table 1, Entry 3**

| Register Address Label | RNW | A0 | A1 | A2 | A3 | | | |
|---|---|---|---|---|---|---|---|---|
| Register Address Bit Stream | 0 | 0 | 0 | 0 | 1 | | | |
| **Line Table Address Label** | **Entry 0** | **Addr 0** | | | | | | |
| Line Table Address Bit Stream | 0000 | 100 | | | | | | |
| **Data Entry Label** | **INTG_STRT Cntl** | **H Bin** | **Enables** | **PBLK Idle** | **Flag** | **Count** | **A0:2** | **A3** |
| Entry 0 Bit Stream | 000 | 00 | 000110000( | 1 | 1 | 0000000000000 | 001 | 0 |
| Entry 1 Bit Stream | 000 | 00 | 000110000( | 1 | 0 | 1000000000000 | 001 | 0 |
| Entry 2 Bit Stream | 000 | 00 | 000110000( | 1 | 0 | 0000000000000 | 01( | 1 |
| Entry 3 Bit Stream | 000 | 00 | 000110000( | 1 | 0 | 0000000000000 | 00( | 0 |

**Table 26 Frame Table 1 Serial Bit Stream**

## Frame Table 2

Frame Table 2 implements the Single Output Full Resolution Capture Mode. Upon completion of the single frame, program execution resumes at the first entry of Frame Table 1. The Idle State configuration of Frame Table 1 allows the imaging system to be reprogrammed for the continuous high speed capture configuration of Frame Table 0.

Entry 0 implements the ExLT command. This entry calls line table 0 which is used to generate the frame transfer pulse. It also clears the vertical line counter. All clamping is disabled in this entry. PBLK is also disabled. Frame Valid and Line Valid are disabled.

| Label | Value | Comment |
|---|---|---|
| Check and Increment Line Counter | 0 | Do not increment Line Counter or compare with INTG_STRT Line Register |
| Clear Line Counter | 1 | Clear Line Counter |
| Force INTG_STRT | 0 | Do not force INTG_STRT |
| Horizontal Binning Factor | 0 | No Binning |
| HCLK_V Enable | 0 | Do not enable HCLKS during Vertical Interval |
| Line Valid Enable | 0 | Disable Line Valid |
| Frame Valid Enable | 0 | Disable Frame Valid |
| Video Amplifier Enable | 1 | Enable Video Amplifier |
| AFE Clock Enable | 1 | Enable AFE Clocks |
| CLPDM2 Enable | 0 | Disable Line Rate clamp |
| CLPDM1 Enable | 0 | Disable Frame Rate clamp |
| CLPOB2 Enable | 0 | Disable Line Rate clamp |
| CLPOB1 Enable | 0 | Disable Frame Rate clamp |
| PBLK Enable | 0 | Disable PBLK |
| PBLK Idle Val | 1 | PBLK active low |
| Flag | 0 | |
| Count | 1 | Execute Line Table 0 once, proceed to next entry when finished |
| Address 2:0 | 0 | |
| Address 3 | 0 | |

**Table 27 Frame Table 2, Entry 0**

Entry 1 is implements the ExLT command again. This entry calls Line Table 1. This line table generates a standard vertical clock sequence that is used to clock out the first dark row. The vertical line counter is enabled for this line. The frame rate clamps and the line rate clamps are disabled. Frame Valid, Line Valid and PBLK are disabled.

| Label | Value | Comment |
|---|---|---|
| Check and Increment Line Counter | 1 | Increment Line Counter and compare with INTG_STRT Line Register |
| Clear Line Counter | 0 | Do not clear Line Counter |
| Force INTG_STRT | 0 | Do not force INTG_STRT |
| Horizontal Binning Factor | 0 | No Binning |
| HCLK_V Enable | 0 | Do not enable HCLKS during Vertical Interval |
| Line Valid Enable | 0 | Disable Line Valid |
| Frame Valid Enable | 0 | Disable Frame Valid |
| Video Amplifier Enable | 1 | Enable Video Amplifier |
| AFE Clock Enable | 1 | Enable AFE Clocks |
| CLPDM2 Enable | 0 | Disable Line Rate clamp |
| CLPDM1 Enable | 0 | Disable Frame Rate clamp |
| CLPOB2 Enable | 0 | Disable Line Rate clamp |
| CLPOB1 Enable | 0 | Disable Frame Rate clamp |
| PBLK Enable | 0 | Disable PBLK |
| PBLK Idle Val | 1 | PBLK active low |
| Flag | 0 | |
| Count | 1 | Execute Line Table 1 1x, proceed to next entry when finished |
| Address 2:0 | 1 | |
| Address 3 | 0 | |

**Table 28 Frame Table 2, Entry 1**

Entry 2 implements the ExLT command. This entry calls Line Table 1. This table generates a standard vertical clock sequence that is used to clock out the 2nd dark row. The vertical line counter is enabled for this line. The frame rate clamps are enabled while the line rate clamps are disabled. Frame Valid, Line Valid and PBLK are disabled.

| Label | Value | Comment |
|---|---|---|
| Check and Increment Line Counter | 1 | Increment Line Counter and compare with INTG_STRT Line Register |
| Clear Line Counter | 0 | Do not clear Line Counter |
| Force INTG_STRT | 0 | Do not force INTG_STRT |
| Horizontal Binning Factor | 0 | No Binning |
| HCLK_V Enable | 0 | Do not enable HCLKS during Vertical Interval |
| Line Valid Enable | 0 | Disable Line Valid |
| Frame Valid Enable | 0 | Disable Frame Valid |
| Video Amplifier Enable | 1 | Enable Video Amplifier |
| AFE Clock Enable | 1 | Enable AFE Clocks |
| CLPDM2 Enable | 0 | Disable Line Rate clamp |
| CLPDM1 Enable | 1 | Enable Frame Rate clamp |
| CLPOB2 Enable | 0 | Disable Line Rate clamp |
| CLPOB1 Enable | 1 | Enable Frame Rate clamp |
| PBLK Enable | 0 | Disable PBLK |
| PBLK Idle Val | 1 | PBLK active low |
| Flag | 0 | |
| Count | 2 | Execute Line Table 1 2x, proceed to next entry when finished |
| Address 2:0 | 1 | |
| Address 3 | 0 | |

**Table 29 Frame Table 2, Entry 2**

Entry 3 is another example of the ExLT command. This entry calls line table 1. This line table generates a standard vertical clock sequence that is used to read out the 4th dark row. Frame rate clamping, Frame Valid, Line Valid, and PBLK disabled. Line rate clamping is enabled. The vertical line counter is enabled.

| Label | Value | Comment |
|---|---|---|
| Check and Increment Line Counter | 1 | Increment Line Counter and compare with INTG_STRT Line Register |
| Clear Line Counter | 0 | Do not clear Line Counter |
| Force INTG_STRT | 0 | Do not force INTG_STRT |
| Horizontal Binning Factor | 0 | No Binning |
| HCLK_V Enable | 0 | Do not enable HCLKS during Vertical Interval |
| Line Valid Enable | 0 | Disable Line Valid |
| Frame Valid Enable | 0 | Disable Frame Valid |
| Video Amplifier Enable | 1 | Enable Video Amplifier |
| AFE Clock Enable | 1 | Enable AFE Clocks |
| CLPDM2 Enable | 1 | Enable Line Rate clamp |
| CLPDM1 Enable | 0 | Disable Frame Rate clamp |
| CLPOB2 Enable | 1 | Enable Line Rate clamp |
| CLPOB1 Enable | 0 | Disable Frame Rate clamp |
| PBLK Enable | 0 | Disable PBLK |
| PBLK Idle Val | 1 | PBLK active low |
| Flag | 0 | |
| Count | 1 | Execute Line Table 1 1x, proceed to next entry when finished |
| Address 2:0 | 1 | |
| Address 3 | 0 | |

**Table 30 Frame Table 2, Entry 3**

Entry 4 implements the ExLT command again. This entry calls Line Table 1 488 times to read out the active video lines. Line rate clamping is enabled while Frame rate clamping is disabled. The vertical line counter is enabled. Frame Valid and Line Valid are enabled. PBLK is disabled.

| Label | Value | Comment |
|---|---|---|
| Check and Increment Line Counter | 1 | Increment Line Counter and compare with INTG_STRT Line Register |
| Clear Line Counter | 0 | Do not clear Line Counter |
| Force INTG_STRT | 0 | Do not force INTG_STRT |
| Horizontal Binning Factor | 0 | No Binning |
| HCLK_V Enable | 0 | Do not enable HCLKS during Vertical Interval |
| Line Valid Enable | 1 | Enable Line Valid |
| Frame Valid Enable | 1 | Enable Frame Valid |
| Video Amplifier Enable | 1 | Enable Video Amplifier |
| AFE Clock Enable | 1 | Enable AFE Clocks |
| CLPDM2 Enable | 1 | Enable Line Rate clamp |
| CLPDM1 Enable | 0 | Disable Frame Rate clamp |
| CLPOB2 Enable | 1 | Enable Line Rate clamp |
| CLPOB1 Enable | 0 | Disable Frame Rate clamp |
| PBLK Enable | 0 | Disable PBLK |
| PBLK Idle Val | 1 | PBLK active low |
| Flag | 0 | |
| Count | 488 | Execute Line Table 1 488x, proceed to next entry when finished |
| Address 2:0 | 1 | |
| Address 3 | 0 | |

**Table 31 Frame Table 2, Entry 4**

Entry 5 implements the JmpFT command. In this case program control is passed back to Frame Table 1 Entry 0.

| Label | Value | Comment |
|---|---|---|
| Check and Increment Line Counter | 0 | Do not increment Line Counter or compare with INTG_STRT Line Register |
| Clear Line Counter | 0 | Do not clear Line Counter |
| Force INTG_STRT | 0 | Do not force INTG_STRT |
| Horizontal Binning Factor | 0 | No Binning |
| HCLK_V Enable | 0 | Do not enable HCLKS during Vertical Interval |
| Line Valid Enable | 0 | Do not Enable Line Valid |
| Frame Valid Enable | 0 | Do not enable Frame Valid |
| Video Amplifier Enable | 1 | Enable Video Amplifier |
| AFE Clock Enable | 1 | Enable AFE Clocks |
| CLPDM2 Enable | 0 | Disable Line Rate clamp |
| CLPDM1 Enable | 0 | Disable Frame Rate clamp |
| CLPOB2 Enable | 0 | Disable Line Rate clamp |
| CLPOB1 Enable | 0 | Disable Frame Rate clamp |
| PBLK Enable | 0 | Set PBLK high |
| PBLK Idle Val | 1 | PBLK active low |
| Flag | 0 | |
| Count | 0 | Jump to Frame Table 1 |
| Address 2:0 | 1 | |
| Address 3 | 0 | |

**Table 32 Frame Table 2, Entry 5**

The serial bit stream for programming Frame Table 2 is shown in Table 33 below.

| Register Address Label | RNW | A0 | A1 | A2 | A3 | | | |
|---|---|---|---|---|---|---|---|---|
| Register Address Bit Stream | 0 | 0 | 0 | 0 | 1 | | | |
| **Line Table Address Label** | **Entry 0** | **Addr 2** | | | | | | |
| Line Table Address Bit Stream | 0000 | 010 | | | | | | |
| **Data Entry Label** | **INTG_STRT Cntl** | **H Bin** | **Enables** | **PBLK Idle** | **Flag** | **Count** | **A0:2** | **A3** |
| Entry 0 Bit Stream | 010 | 00 | 000110000( | 1 | 0 | 1000000000000 | 00( | 0 |
| Entry 1 Bit Stream | 100 | 00 | 000110000( | 1 | 0 | 1000000000000 | 10( | 0 |
| Entry 2 Bit Stream | 100 | 00 | 000110101( | 1 | 0 | 0100000000000 | 10( | 0 |
| Entry 3 Bit Stream | 100 | 00 | 000111010( | 1 | 0 | 1000000000000 | 10( | 0 |
| Entry 4 Bit Stream | 100 | 00 | 011111010( | 1 | 0 | 0001011110000 | 10( | 0 |
| Entry 5 Bit Stream | 000 | 00 | 000110000( | 1 | 0 | 0000000000000 | 10( | 0 |

**Table 33 Frame Table 2 Serial Bit Stream**

## FLUSH IMPLEMENTATION

The KSC-1000 can easily be programmed to flush the KAI-0340 image sensor. The vertical clock pulse width and the duration between vertical clock pulses are defined in the line table. The HCLK_V Enable bit is set in the frame table entry in which the flush line table is called. This allows the horizontal clocks to run during the vertical interval time. The HCLK_H Enable bit in the line table is not set in the last entry. This prevents the KSC-1000 from entering the horizontal readout state and causes the flush line table to be executed repeatedly until the termination condition for the frame table entry is satisfied. Table 34 below is an example of a fast flush implementation that generates vertical clock pulses every 400nS.

| Entry | Label | Value | Time | Comment |
|---|---|---|---|---|
| 0 | Count | 8 | 200nS | 8 25nS clock periods required for 200nS pulse |
| 0 | HCLK_H | 0 | | Set to 0, not last active entry in the line table |
| 0 | V6 | 0 | | FD low |
| 0 | V5 | 0 | | V2C High-Mid driver at mid level |
| 0 | V4 | 1 | | V2C driver at mid level |
| 0 | V3 | 0 | | V2 High-Mid driver at mid level |
| 0 | V2 | 1 | | V2 driver at mid level |
| 0 | V1 | 0 | | V1 driver at low level |
| 1 | Count | 8 | 200nS | 8 25nS clock periods required for 200nS period |
| 1 | HCLK_H | 0 | | Do not proceed to horizontal readout upon completion of line table |
| 1 | V6 | 0 | | FD low |
| 1 | V5 | 0 | | V2C High-Mid driver at mid level |
| 1 | V4 | 0 | | V2C driver at low level |
| 1 | V3 | 0 | | V2 High-Mid driver at mid level |
| 1 | V2 | 0 | | V2 driver at low level |
| 1 | V1 | 1 | | V1 driver at mid level |
| 2 | Count | 0 | | All zero entry to indicate end of line table |
| 2 | HCLK_H | 0 | | |
| 2 | V6 | 0 | | |
| 2 | V5 | 0 | | |
| 2 | V4 | 0 | | |
| 2 | V3 | 0 | | |
| 2 | V2 | 0 | | |
| 2 | V1 | 0 | | |

**Table 34 Fast Flush Line Table**

## LINE RATE ELECTRONIC SHUTTERING

The Force INTG_STRT bit can be used to implement line rate electronic shuttering. This bit is set for those frame table entries in which line rate electronic shuttering is desired. Since the INTG_STRT timing sequence is executed before the line table, each line in which the Force INTG_STRT bit is set will be lengthened by the duration of the INTG_STRT setup, pulse, and hold times.

## EXTENDED INTEGRATION TIME

Integration time can easily be extended beyond the frame readout time. After completion of the frame readout an ExLTNVD instruction can be used to extend the integration time indefinitely. The line table could either park the vertical clocks in their idle state or continue the image frame readout clocking to over-clock the sensor. Horizontal clocks could optionally be disabled to save power. This approach requires the system controller to provide a VD signal to terminate the integration period.

Integration time can also be extended without the use of the VD signal by changing the count field of a Frame Table entry. A line table can be configured as integration time minimum unit and called repeatedly to create the desired integration time.

## GENERAL PURPOSE REGISTERS

There are 8 General Purpose Registers. The functionality of these registers are detailed in the KSC-1000 Device Performance Specification. The programming of the General Setup Register, along with the INTG_STRT Setup Register, and the INTG_STRT Line Register are described below.

### General Setup Register

The values programmed in the General Setup Register are application dependent. For purposes of the discussion below, the following assumptions are made:

1. There is no over clocking of the horizontal shift register
2. It is desired to store only the active pixels
3. Line rate clamping occurs on the leading dark pixels
4. The CLPDM and CLPOB signals start and stop at the same pixel locations

The value programmed in the Pixels Per Line field is dependent upon the mode of image sensor operation. A value of 708 is required to for the Single Output Full Image Capture configured with Frame Table 2. A value of 246 is required for the Single Output Center Rows and Columns Readout mode configured in Frame Table 0.

The Line Valid signal is typically used as a sync signal by an external framestore. For the Single Output Full Image Capture mode, the Line Valid Pixel Start field is programmed to a value of 36. This causes the 12 leading dummy pixels and the 24 leading dark pixels to be discarded by the framestore. The Line Valid Pixel End field is programmed to a value of 664. This will discard the 24 trailing dark pixels. For Single Output Center Rows and Columns Readout mode, the Line Valid Pixel Start field is programmed to a value of 0. There are no leading dark or dummy pixels in this mode. The Line Valid Pixel End field is programmed to a value of 228 to discard the 18 over clocked pixels at the end of the line.

CLPOB_1 and CLPDM_1 are used for frame rate clamping. For the Single Output Full Image Capture mode, a value of 14 is programmed to the CLPDM_1 Pixel Start and CLPOB_1 Pixel Start fields. The CLPOB_1 Pixel End and CLPDM_1 Pixel End fields are programmed to a value of 706. For Single Output Center Rows and Columns Readout mode, a value of 2 is programmed to the CLPDM_1 Pixel Start and CLPOB_1 Pixel Start fields. The CLPOB_1 Pixel End and CLPDM_1 Pixel End fields are programmed to a value of 244. These selections allow clamping on the entire dark row with the exception of 2 pixels on either edge.

CLPOB_2 and CLPDM_2 are used for line rate clamping. For the Single Output Full Image Capture mode, a value of 14 is programmed to the CLPDM_2 Pixel Start and CLPOB_2 Pixel Start fields. The CLPOB_2 Pixel End and CLPDM_2 Pixel End fields are programmed to a value of 34. These selections allow clamping on the leading dark pixels with the exception of the 2 edge pixels. For Single Output Center Rows and Columns Readout mode, a value of 230 is programmed to the CLPDM_2 Pixel Start and CLPOB_2 Pixel Start fields. The CLPOB_2 Pixel End and CLPDM_2 Pixel End fields are programmed to a value of 244. These selections allow clamping on the trailing over clocked pixels with the exception of the 2 boundary pixels on either side.

PBLK is typically used to provide a blanking signal during the vertical clocking interval. For this application, the PBLK Pixel Start field is programmed the value in the Pixels Per Line field. The PBLK Pixel End field is programmed to a value of 0.

There are 14 enable bits for the all of the pixel clock rate outputs. For this example, the following assumptions regarding the pixel rate output clocks are made. 2 horizontal clock signals are required to implement a single channel output design. H1 and H2 are used for the horizontal clocks. SH1, SH2, and DATACLK1 are used to drive the AFE chip. DATACLK2 is used to clock image data into an external image memory.

There are 13 24mA enable bits for all of the pixel rate outputs with the exception of PIXCLK. The 24mA drive selection provides faster rise and fall times. For this example, it is assumed that the 12mA drive is used for all of the selected outputs.

Finally, there are 4 bits to select the proper DLL for the desired pixel clock frequency. DLL 10 is chosen for the 40MHz pixel clock frequency.

The bit stream for register 1 configured for Single Output Center Rows and Columns mode is shown in Table 35 below.

| Label | Bit Field Width | Data | Bit Stream |
|---|---|---|---|
| Register Address | 5 | 2 | 01000 |
| Pixels Per Line | 13 | 246 | 0110111100000 |
| Line Valid Pixel Start | | 0 | 0000000000000 |
| Line Valid Pixel Quadrature Start | 2 | 0 | 00 |
| Line Valid Pixel End | 13 | 228 | 0010011100000 |
| CLPOB1_Pix_Start | 13 | 2 | 0100000000000 |
| CLPOB1_Pix_End | 13 | 244 | 0010111100000 |
| CLPOB2_Pix_Start | 13 | 230 | |
| CLPOB2_Pix_End | 13 | 244 | 0010111100000 |
| CLPDM1_Pix_Start | 13 | 2 | |
| CLPDM1_Pix_End | 13 | 244 | 0010111100000 |
| CLPDM2_Pix_Start | 13 | 230 | |
| CLPDM2_Pix_End | 13 | 244 | 0010111100000 |
| PBLK_Pix_Start | 13 | 246 | |
| PBLK_Pix_End | 13 | 0 | 0000000000000 |
| Pixel Rate Clock Enable Bits | 14 | | |
| Pixel Rate Clock 24mA Drive Enable Bits | 13 | | 0001101101110 |
| DLL Select Bits | 4 | 10 | |

**Table 35 General Setup Register Serial Bit Stream**

## INTG_STRT Setup Register

The KSC-1000 inserts a shutter pulse after the end the horizontal readout and before the start of the vertical clocking interval. Electronic Shutter timing requirements for the KAI-0340 are shown in Figure 5.

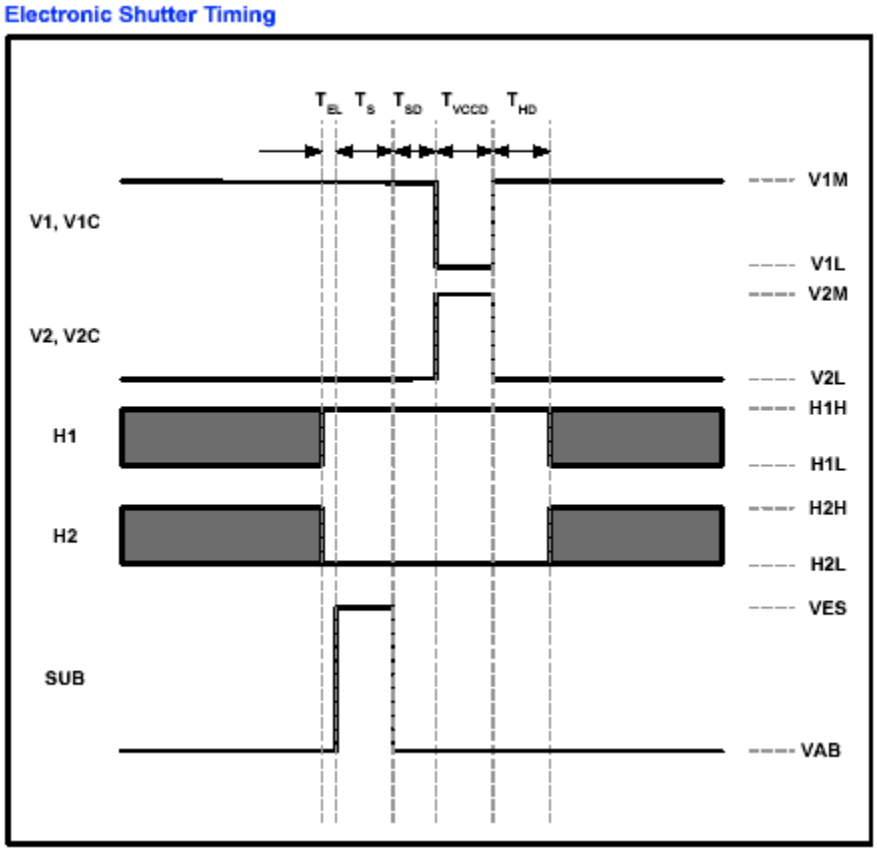


**Figure 5 KAI-0340 Electronic Shutter Timing**

Referring to Timing Requirements in Table 2 on page 6, the KAI-0340 requires a shutter pulse of 1uS and a shutter pulse delay of 1uS. With a 25nS pixel clock period, 40 pixel clocks are required to generate a 1uS period. A single pixel clock delay is required for shutter setup time.

Table 24 is a register map of the INTG_STRT Setup Register.

| Label | Value | Time | Comment |
|---|---|---|---|
| INTG_STRT Setup Time | 1 | 25nS | 1 25nS clock period required for 25nS Setup Time |
| INTG_STRT Pulse Width | 40 | 1uS | 40 25nS clock periods required for 1uS Pulse Width |
| INTG_STRT Hold Time | 40 | 1uS | 40 25nS clock periods required for 1uS Hold Time |

**Table 36 INTG_STRT Setup Register Map**

Table 25 illustrates the serial bit stream required to program the INTG_STRT register with the values shown in Table 24. The register fields are programmed from top to bottom as listed in the KSC-1000 Device Performance Specification. Each register field must be programmed with the LSB first. This format holds true for all of the General Purpose Registers.

| Register Address Label | RNW | A0 | A1 | A2 | A3 |
|---|---|---|---|---|---|
| Register Address Bit Stream | 0 | 1 | 1 | 0 | 0 |
| **Data Entry Label** | **INTG_STRT Setup** | **INTG_STRT Pulse Width** | | | |
| Bit Stream | 1000000000 | 0001010000 | 0001010000 | | |

**Table 37 INTG_STRT Register Serial Bit Stream**

## INTG_STRT Line Register

The value in the INTG_STRT Line register is compared to the vertical line counter. When a match occurs the INTG_STRT signal is inserted prior to the vertical interval. Proper management of counter incrementing and clearing in the line tables is required to produce the expected results.

## REVISION CHANGES

| Revision Number | Description of Changes |
|---|---|
| 1.0 | Initial release |

**Table 38 Revision History**